IN THE CLAIMS:

Please amend claims 1, 3, 4, 9-11, 13-16, 18-20, 27, 29, and 31-33 as follows:

1 (2nd amended). A semiconductor device, comprising:

a semiconductor substrate having a circuit area where an integrated circuit is formed and a peripheral area where an integrated circuit is not formed, the peripheral area surrounding the circuit area;

wiring patterns formed on the substrate in the circuit area;

a first dummy pattern which is formed of the same material as the wiring pattern, formed in the peripheral area, the dummy pattern encompassing the circuit area;

a first insulating layer formed on the circuit area and the peripheral area of the semiconductor substrate;

a second insulating layer formed on the first insulating layer which is formed on the semiconductor substrate, wherein the second insulating layer is formed over the wiring patterns, and the second insulating layer is not formed over the first dummy pattern; and

a third insulating layer formed on the exposed first insulating layer and the second insulating layer.

3 (2nd amended). A semiconductor device as claimed in claim 2, wherein the SOG layer has a certain concentration of solid content, and the first dummy pattern has a width, which is determined by the concentration of solid content of the SOG layer.

4 (2nd amended). A semiconductor device as claimed in claim 2, wherein the first dummy pattern has a width, which is less than 1 μm, and a concentration of solid content of the SOG layer is around 5.2 wt%.

9 (1st amended). A semiconductor device as claimed in claim 8, wherein the SOG layer has a certain concentration of solid content, and each of the first and second dummy patterns has a width, which is determined by the a concentration of solid content of the SOG.

10 (2nd amended). A semiconductor device as claimed in claim 8, wherein each of the first and second dummy patterns has a width, which is less than 1 μm, and a concentration of solid content of the SOG layer is around 5.2 wt%.

11 (2nd amended). A semiconductor device as claimed in claim 1, further comprising:

a third dummy pattern formed in the peripheral area between the first dummy pattern and the wiring patterns, the second insulating layer being not formed on the third dummy pattern.

13 (2nd amended). A semiconductor device as claimed in claim 11, wherein the distance between the first dummy pattern and the third dummy pattern exceeds 0.9 μm.

14 (2nd amended). A semiconductor device as claimed in claim 11, wherein the second insulating layer is a SOG layer, the SOG layer has a certain concentration of solid content, and each of the first and third dummy layer has a width, which is determined by the concentration of solid content of the SOG layer.

15 (2nd amended). A semiconductor device as claimed in claim 11, wherein the second insulating layer is a SOG layer, each of the first and third dummy layer has a width, which is less than 1 μm, and a concentration of solid content of the SOG layer is around 5.2 wt%.

16 (2nd amended). A semiconductor device as claimed in claim 1, further comprising:

a bonding pad formed on the semiconductor substrate in the circuit area; and

a fourth dummy pattern, which is connected to the first dummy pattern, the second insulating layer being not formed on the fourth dummy layer,

wherein the bonding pad is surrounded by the first and fourth dummy patterns.

18 (1st amended). A semiconductor device as claimed in claim 16, wherein a distance between the fourth dummy pattern and the bonding pad exceeds 0.9 μm.

19 (2nd amended). A semiconductor device as claimed in claim 16, wherein the second insulating layer is a SOG layer, the SOG layer has a certain concentration of solid content, and each of the first and fourth dummy layer has a width, which is determined by the concentration of solid content of the SOG layer

20 (2nd amended). A semiconductor device as claimed in claim 16, wherein each of the first and fourth dummy layer has a width, which is less than 1 μm, and a concentration of solid content of the SOG layer is around 5.2 wt%.

27 (1st amended). A semiconductor device, comprising:

a semiconductor substrate having a circuit area where an integrated circuit is formed and a peripheral area where an integrated circuit is not formed, the peripheral area surrounding the circuit area;

wiring patterns formed on the substrate in the circuit area;

a dummy pattern which is formed of the same material as the wiring pattern, formed in the peripheral area, the dummy pattern encompassing the circuit area; and

an insulating layer formed above the semiconductor substrate, the insulating layer being formed over the wiring patterns, the insulating layer being formed outside the dummy pattern but not being formed over the dummy pattern, and the insulating layer having a moisture absorbable characteristic.

29 (1st amended). A semiconductor device, comprising:

a semiconductor substrate having a circuit area where an integrated circuit is formed and a peripheral area where an integrated circuit is not formed, the peripheral area surrounding the circuit area;

wiring patterns formed on the substrate in the circuit area, the wiring pattern including a pad pattern;

a dummy pattern which is formed of the same material as the wiring pattern, formed in the peripheral area, the dummy pattern encompassing the circuit area;

a first insulating layer formed over the wiring patterns and the dummy pattern, an edge of the first insulating layer being located on the pad pattern, which is adjacent the dummy pattern; and

a second insulating layer formed above the semiconductor substrate, the second insulating layer being formed over the wiring patterns and the second

insulating layer being formed outside the dummy pattern but not being formed over the dummy pattern.

31 (1st amended). A semiconductor device as claimed in claim 1, wherein the wiring patterns include a pad pattern, the edge of the first insulating layer being located on the pad pattern which is adjacent to the dummy pattern.

32 (1st amended). A semiconductor device as claimed in claim 30, wherein the wiring patterns include a pad pattern, the edge of the first insulating layer being located on the pad pattern which is adjacent to the dummy pattern.

33 (1st amended). A semiconductor device as claimed in claim 29, wherein the second insulating layer has a moisture absorbable characteristic.

REMARKS

The Examiner's Office Action of June 11, 2002 has been received and carefully reviewed. Claims 1, 3, 4, 9-11, 13-16, 18-20, 27, 29, and 31-33 are amended. Claims 21-26 have been withdrawn from consideration. Thus, claims 1-20 and 27-33 are pending in this application. For at least the following reasons,